Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches

With the support by the National Natural Science Foundation of China, the research team led by Prof. Peng LianMao (彭练矛) and Prof. Zhang ZhiYong (张志勇) at the Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing, recently reported Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches, in *Science* (2018, 361: 387—392).

An efficient way to reduce the power is to lower the supply voltage VDD, but this voltage is restricted by the 60 millivolts per decade thermionic limit of subthreshold swing (SS) in field-effect transistors (FETs). They show that a graphene Dirac source (GDS) with a much narrower electron density distribution around the Fermi level than that of conventional FETs can lower SS. A DS-FET with a carbon nanotube channel provided an average SS of 40 millivolt per decade over four decades of current at room temperature and high device current I60 of up to 40 microampere per micrometer at 60 millivolts per decade. When compared with state-of-the-art Si 14-nanometer node FETs, a similar Ion is realized but at much lower supply voltage of 0.5 versus 0.7 volts for Si, and a much steeper SS below 35 millivolts per decade in the off-state.

In principle, the graphene Dirac source may also be combined with other semiconductor channel materials, e. g. semiconducting nanowires, 2D or even conventional bulk semiconductors, to simultaneously achieve sub-60 mV/decade SS and high I_{on}. The DS-FET may thus be used as a general device or building block for future ICs with sub-0.5 V power-supply.

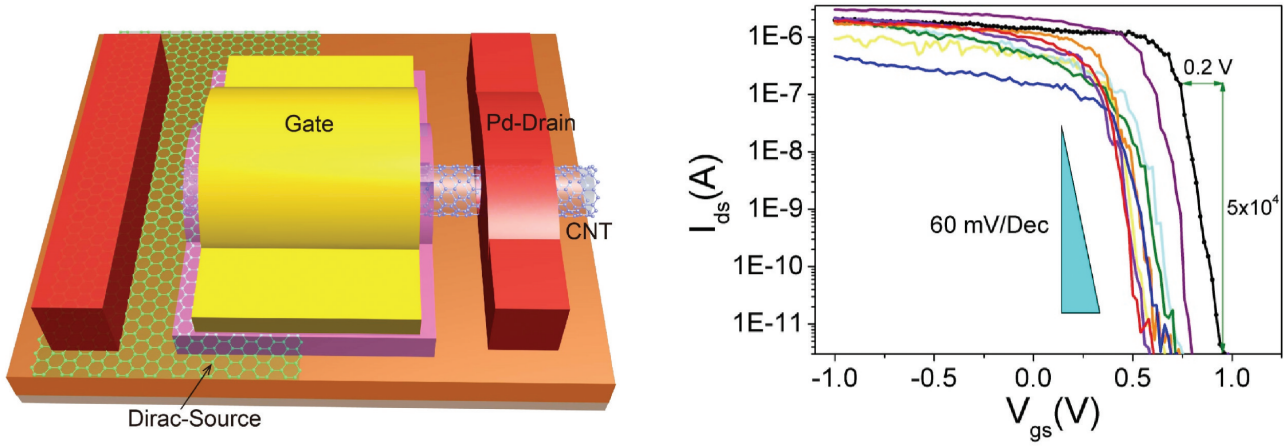

Figure Schematic diagram and performance of CNT CMOS FETs, showing that CNT CMOS FETs are 10 times better than Si CMOS on speed and power dissipation comprehensively.